Remarks

By this Supplementing Amendment, additional revisions are being implemented in the claims that are, basically, of an editorially further clarifying nature. These revisions are being implemented as a result of a further follow-up consideration given of the file history of the above-identified application. In addition to effecting further clarification as well as removing a discovered duplicate expression, several grammatical and other minor revisions are also being implemented.

With regard to independent claim 1, the paragraph formatting therein is being revised so as to avoid using the punctuation mark ":" more than a single instance within that claim and, moreover, to more clearly list the constituent components of the claimed subject matter associated with the respective zener diodes (see subparagraph (i) – (iii)). Several other clarifications were effected, also, in claim 1 that should be clearly evident from a careful reading thereof. For example, in the subparagraph "a plurality of first connection holes ... and a plurality of second connection holes ... formed in said insulation film," a revision is being effected to more clearly state that the "first connection holes" are for providing electrical connections therethrough to the first semiconductor region and that the "second connection holes" are for providing electrical connections therethrough to the well region, as can be seen with regard to Figs. 3-5 of the drawings, as one example. With regard to Fig. 4, it is noted that the first connection holes (e.g., connection holes 24) are extended through the silicon oxide insulator 29 to expose the first semiconductor region (e.g., n^+ region 20) while the second connection holes (e.g., 25) are extended through the insulator 29 to expose the well region (e.g., p well 5 via the p^+ ohmic contact 19).

With regard to the "wherein" clause in the last subparagraph of base claim 1, a correction was effected therein to remove a discovered typographical error as well as to editorially clarify that the first connection holes provide electrical connections therethrough between the first semiconductor region and the wiring. In the example embodiment shown in Fig. 4 of the drawings, the wiring includes a wire 22 which is formed over the insulating film 29 and which connects the first connection holes (e.g., 24 associated with zener diode D2) and the second connection holes 25 associated with the second zener diode (e.g., D1). Moreover, it is noted that the first connection holes (e.g., 24 in Figs. 3 and 4) provide electrical connections therethrough between the first semiconductor region (e.g., n^+ region 20) and the wiring (e.g., wire 22). Although such intent is obvious from the previously existing language, it has now been somewhat further clarified to avoid any possible question of intent. Insofar as applicable, similar revisions were also implemented with regard to other ones of the independent claims, including claims 29, 32 and 36.

With regard to independent claim 29, moreover, a previously existing expression which was intended to be removed (since it was re-presented as a newly added dependent claim 38) with the filing of the Amendment of December 23, 2002, was discovered to still remain therein. Accordingly, it is presently being deleted so as to avoid duplicate claim language with that in claim 38. A minor grammatical correction is being effected, also, in line 2 of claim 29. With regard to independent claim 36, in the "wherein" clause thereof, several grammatical corrections are being effected therein and, moreover, the expression "semiconductor region" is being appropriately revised to that of second semiconductor region, as should be clearly apparent. Finally, with

regard to dependent claim 35, the expression "second semiconductor region" at the end of that claim is being reverted to that of first semiconductor region, as should be clearly apparent. That is, as can be seen from independent claim 32 thereof, insofar as applicable to the Fig. 4 illustration, although not limited thereto, the "first semiconductor region of said first conductivity type" relates to n^+ region 20 and the "second semiconductor region of said second conductivity type" relates to the underlying p region 6. Also according to independent claim 32, the "first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said second semiconductor region is not formed." As can be seen from Fig. 4, the shown upper n^+ region 20 has an outer periphery portion surrounding P region 6 and, consistent with dependent claim 35, the junction depth of the first portion of n^+ region 20 is shallower than that of the second portion.

In connection with the further review made of the present specification, an incorrect reference number was noted with regard to Fig. 4 of the drawings. Accordingly, enclosed herewith is a paper entitled, "Request for Approval to Amend the Drawings," seeking approval to correct the noted informality. Namely, the connection holes 24 which are extended through the insulator 29 to expose the n^+ region 20 of each of the diodes D1 and D2 is improperly labeled as connection hole 25 on the illustrated right side periphery portion of region 20 associated with the diode D2 section of the illustration. Incidentally, connection holes 25 are those extended through the insulator 29 to expose the P wells 6. This is also confirmed with regard to Figs. 3 and 5, which relate to the cross-sectional showing of Fig. 4. This noted informality in Fig. 4 will be formally

corrected upon approval thereof of the accompanying request directed thereto. That is, correction of this drawing informality will be implemented at such time as subsequently to applicants receiving a formal Notification of Allowability of the above application.

As explained above, the additional amendments presented hereinabove are, basically, of a further editorially clarifying nature including also changes to correct obvious informalities that were discovered during a further review thereof. Accordingly, it is respectfully requested that this Amendment be accepted and formally entered as a supplement to the earlier filed fully responsive Amendment of December 23, 2002.

Applicants, through their undersigned representative, would like to make of note also the following additional clarification. With regard to the responsive amendment of December 23, 2002, in the Remarks thereof, on page 11 of that Amendment, the second sentence thereof is partly misdescriptive. It instead should read as follows:

Regarding canceled claim 28, the first and second parts thereof were incorporated into that of base claim 1, the third part thereof is contained in dependent claim 27 ... and the last part thereof relating to the wiring is now contained in amended claim 1.

Accordingly, the Examiner is asked to note the above correction to that sentence of the earlier submitted responsive amendment when reviewing the same.

It is requested that the additional amendments presented hereinabove be entered accordingly and duly considered together with the earlier filed responsive amendment of December 23, 2002. Moreover, for the same and similar reasons as that argued in the remarks of that earlier responsive amendment and in view of the additional amendments presented hereinabove, together with these further clarifying remarks, reconsideration and withdrawal of

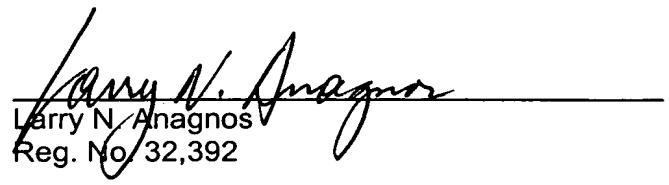
all of the previously standing rejections as well as a favorable action therefor on the presently pending claims, i.e., claims 1-3, 22 and 24-38, directed to the previously elected invention, and an early formal notification of Allowability of the above-identified application is respectfully requested.

A marked-up version showing changes made is enclosed herewith.

If the Examiner deems that questions and/or issues still remain which would prevent the present application from being allowed at the present time, he is urgently invited to telephone the undersigned representative, at the number indicated below, so that either a telephone or personal interview may be arranged at the Examiner's convenience in order to discuss the same and hopefully resolve any remaining questions/issues present.

If any fees are due in connection with the filing of this paper, please charge the same to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (843.39542X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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MARKED-UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS:

Please **amend** claims 1, 29, 32, 35 and 36, as follows:

1. **(Four Times Amended)** A semiconductor integrated circuit device comprising:

a semiconductor substrate of a second conductivity type;

at least two or more two zener diodes connected in series each comprised of[:]

(i) a well region of a first conductivity type formed on said semiconductor substrate[;],

(ii) a first semiconductor region of said second conductivity type formed in said well region[;] , and

(iii) a second semiconductor region of said first conductivity type formed in said well region at a bottom portion of said first semiconductor region and being smaller in area, defined by a planar pattern thereof, than said first semiconductor region[,];

an insulation film formed over a primary face of said semiconductor substrate; [and]

a plurality of first connection holes for [electrically connecting] providing electrical connections therethrough to said first semiconductor region and a plurality of second connection holes for [electrically connecting] providing

electrical connections therethrough to said well region[, both of which are] being formed in said insulation film; and

wherein a wiring is formed over said insulation film and [electrically] connecting [with] said first connection holes of a first of said zener diodes and said second connection holes of a second of said zener diodes, said plurality of first connection holes[, for electrically connecting] provide electrical connections therethrough between said first semiconductor region and [a wire to each other,] said wiring and are arranged in a region located outside a junction formed between said first semiconductor region and said second semiconductor region of said first zener diode, a first PN junction formed between said first semiconductor region and said second semiconductor region functions as a diode device, and a second PN junction is formed between said semiconductor substrate and said well region and has a breakdown voltage greater than that of said first PN junction .

29. **(Twice Amended)** A semiconductor integrated circuit device comprising:

a first diode and a second diode [connecting] connected in series, each of said first and second [diode] diodes including[:]

(i) a first semiconductor region of a first conductivity type being formed in a semiconductor substrate[;],

(ii) a second semiconductor region of a second conductivity type, the second semiconductor region being formed in said first semiconductor region[;], and

(iii) a third semiconductor region of a first conductivity type, the third semiconductor region being formed in said first semiconductor region and under said second semiconductor region; [and]

an insulation film formed over a primary face of said semiconductor substrate; [and]

a plurality of first connection holes for [electrically connecting] providing electrical connections therethrough to said second semiconductor region and a plurality of second connection holes for [electrically connecting] providing electrical connections therethrough to said first semiconductor region[, both of which are] being formed in said insulation film[,]; and

wherein a wiring is formed over said insulation film and [electrically] connecting said first connection holes associated with said first diode and said second connection holes associated with said second diode, a first PN junction formed between said second semiconductor region and said third semiconductor region functions as a diode device, [said third semiconductor region has an impurity concentration higher than that of said first semiconductor region,] said second semiconductor region has a first portion and a second portion, the first portion is that in which a PN junction is formed between said third semiconductor region and said second semiconductor region and the second portion is that below which said third semiconductor region is not formed, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed outside said first portion, and said first connection holes are formed over said second portion of said second semiconductor region.

32. **(Twice Amended)** A semiconductor integrated circuit device comprising:

a first well region of a first conductivity type being formed in a semiconductor substrate;

a second well region of a second conductivity type being formed in said first well region;

a first semiconductor region of said first conductivity type, the first semiconductor region being formed in said second well region;

a second semiconductor region of said second conductivity type, the second semiconductor region being formed in said second well region under said first semiconductor region; and

an insulation film formed over a primary face of said semiconductor substrate and having a plurality of first connection holes for [electrically connecting] providing electrical connections therethrough between said first semiconductor region and wiring,

wherein said first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said second semiconductor region is not formed, a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and functions as a diode device, said second portion is formed outside said first portion, said first connection holes are formed over said second portion of said first semiconductor region, and second semiconductor region has an impurity concentration higher than that of said second well region, and a second PN

junction is formed between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.

35. **(Amended)** A semiconductor integrated circuit device according to claim 33, wherein a junction depth of said first portion of said first semiconductor region is shallower than that of said second portion of said [second] first semiconductor region.

36. **(Twice Amended)** A semiconductor integrated circuit device comprising:

a first diode and a second diode connected in series and formed in a first well region, the first well region being formed on a semiconductor substrate, said first diode and said second diode, respectively, comprising[:]

(i) a second well region of a first conductivity type, the second well region being formed in said first well region which is of a second conductivity type[;],

(ii) a first semiconductor region of a second conductivity type, the first semiconductor region being formed in said second well region[;], and

(iii) a second semiconductor region of a first conductivity type, the second semiconductor region being formed in said second well region and under said first semiconductor region; [and]

an insulation film formed over a primary face of said semiconductor substrate; [and]

a plurality of first connection holes for [electrically connecting] providing electrical connections therethrough to said first semiconductor region and a

plurality of second connection holes for [electrically connecting] providing electrical connections therethrough to said second well region[, both of which are] being formed in said insulation film[,]; and

wherein a wiring formed on said insulation film and [connection with] connecting said first connection holes in said first diode and said second connection holes in said second diode, said second semiconductor region has an impurity concentration higher than that of said second well region, said first semiconductor region has a first portion and a second portion, the first portion is that below which said second semiconductor region is formed and the second portion is that below which said second semiconductor region is not formed, a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and constitutes a zener diode, a junction depth of said first portion is shallower than that of said second portion, said second portion is formed in a periphery of said first portion so as to surround said first portion, said plurality of first connection holes are arranged over said second portion so as to surround said first portion, and a second PN junction is formed between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.